



Silicon Dreams
S I L I C O N T O T H E P O W E R O F Y O U R D R E A M S

eMMC 5.1 PHY

Datasheet

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1 Introduction

Silicon Dreams is a provider of licensable Intellectual Property Cores for the Semiconductor industry along with software development and SoC design services.

Silicon Dreams was founded in 2022 to address the burgeoning semiconductor industry and its timing was well founded with the company's explosive growth along with the AI boom. The company is rapidly expanding its operations internationally to be closer to its customer base.

We have licensees Worldwide with most of our customers based in the USA followed by the APAC region with a significant presence in China and Japan.

Our goal is to enable customers to realize their dreams on silicon through our licensable intellectual property cores, design services and software.

The company can also build custom silicon per the customers specifications.

2 eMMC 5.1 Host PHY Datsheet

2.1 Overview

The eMMC5.1 PHY is to be fully compliant PHY layer for JEDEC eMMC5.1 when rectified and eMMC5.1 JESD84-B50 specification. It is backward compliant with eMMC4.51 and earlier versions of the specifications. This allows the designers of the SOC to easily support the EMMC interface and optimize the performance and power while maintaining interoperability with eMMC5.0 and eMMC5.1 devices.

2.2 Features

The following are the high level features of the eMMC5.1 PHY:

- Designed for seamless integration with eMMC5.1 Host Controller.
- Supports HS400, HS200, DDR50 and legacy operating modes.
- Includes EMMC I/O PADS with ESD protection structures.
- The EMMC I/O PADS are designed to meet eMMC5.1 HS400 specifications.
- Integrate a Master Slave DLL for tuning the Receive clock (in HS200), STRB (in HS400) modes.
- Delay Chain based clock tuning for TX Clock, RX Clock and STRB Clock.
- Built-in diagnostics for monitoring the DLL.
- eMMC5.1 PHY is available in the following TSMC technology nodes:
 - 16nm FF plus v1.0 process (GL and LL)
 - 28nm HPM, HPC and LP
 - 40nm LP
- The design is intended for core supply V_{CORE} +/-10% and I/O supply V_{CCQ} +/-10%.

2.3 Architecture

2.3.1 1HS400 Overview

This Silicon dreams IP consists of hardened PHY IP and RTL block code. The hard-macro consists of analogIPs, such as eMMC 5.1 interface Pads, Impedance Calibration Pad, an analog DLL, and the DLL wrapper. The RTL Block code includes Host/Device controller.

To assist with eMMC 5.1 IP integration, Silicon Dreams provides all of the back-end views of eMMC 5.1 GPIO Pads and CALIO Pad integrated with TSMC ESD protection structure for I/O VDDQ, VSSQ and Power Clamps.

The eMMC5.1 PHY consists of two major sections DFE and an AFE.

The eMMC5.1 PHY DFE Contains:

- The interface.to eMMC5.1 Host Controller and Main SOC command processor

- The Host Controller supports HS400, HS200, DDR50 and legacy data rates.
- Includes the Input / Output flops to support both SDR and DDR operation on the Data Lines. Thus alleviating the timing responsibilities from the eMMC5.1 Host Controller.
- Includes the DLL clocks phase selection and MUXING logic.
- Includes data buffering FIFO and EMMC I/O data synchronizing Flops.

The eMMC5.1 PHY AFE contains:

- EMMC PADS with integrated ESD protection {CMD line, DAT [0:7] lines, CLK line and STRB line}.
- CALIO PAD to automatically calibrate the source and sink impedance of EMMC I/O.
- Analog DLL to provide the following functionality.
- Generates 32 phases equally spaced of STRB for data shifting in HS400 (for reads).
- Generates 32 phases equally spaced of RX clock for Tuning function in the HS200 and HS400 mode of operation.
- Generates 32 phases equally spaced of TX clock for Tuning to support various hold requirements on the EMMC CMD/DAT lines at various mode of operation.
- The DLL clock frequency can be programmed to support any constant clock frequency in the range of 50MHz to 275MHz.

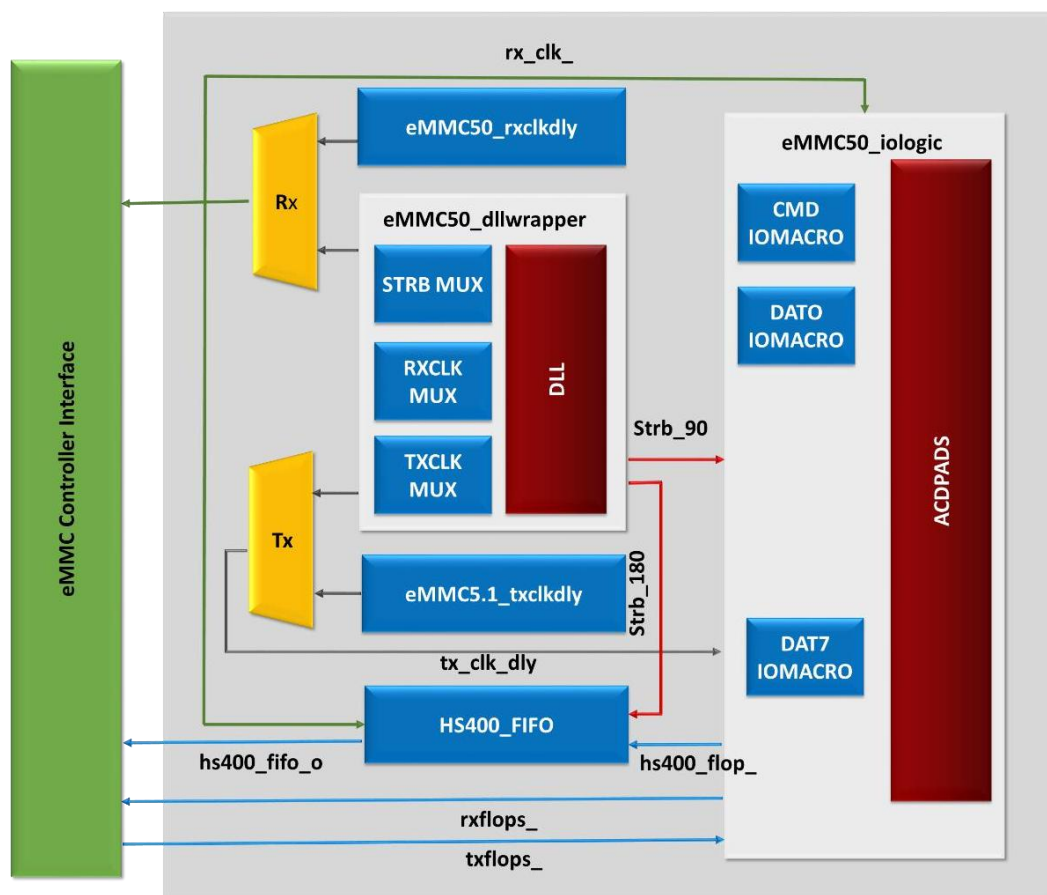


Figure 3 - HS400 Block Diagram

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2.4 Deliverables

- GDSII database
- LVS Netlist
- Physical Abstract Model (LEF)
- Timing Models
- Behavioral Models
- Design Integration Guide
- Technical Documents