



Silicon Dreams
S I L I C O N T O T H E P O W E R O F Y O U R D R E A M S

eMMC 5.1 Host Controller IP

Datasheet

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1 Introduction

Silicon Dreams is a provider of licensable Intellectual Property Cores for the Semiconductor industry along with software development and SoC design services.

Silicon Dreams was founded in 2022 to address the burgeoning semiconductor industry and its timing was well founded with the company's explosive growth along with the AI boom. The company is rapidly expanding its operations internationally to be closer to its customer base.

We have licensees Worldwide with most of our customers based in the USA followed by the APAC region with a significant presence in China and Japan.

Our goal is to enable customers to realize their dreams on silicon through our licensable intellectual property cores, design services and software.

The company can also build custom silicon per the customers specifications.

2 eMMC 5.1 Host Controller Datasheet

2.1 Overview

Silicon Dreams eMMC5.1 Host Controller IP is a highly integrated Intellectual Property (IP) solution that supports three key memory and I/O technologies:

1. JEDEC eMMC (eMMC Multi Media Card) 5.1 (Draft)
2. JEDEC eMMC CQHCI for Command Queueing
3. SDA Secured Digital (SD) 3.01
4. SDA Secured Digital Input Output (SDIO) 3.01

This IP handles all the timing and interface protocol requirements to access these media as well as processing the commands in hardware.

The IP supports connection to a single slot and performs multi-block writes and erases that lower access overhead. In addition, a host can utilize this IP to boot directly from an attached eMMC device, thereby simplifying system initialization during power up. The host interface is based on a standard 32-bit/64-bit Advanced High-Performance Bus (AHB/AXI/OCP) which is used to transfer data and configure the IP.

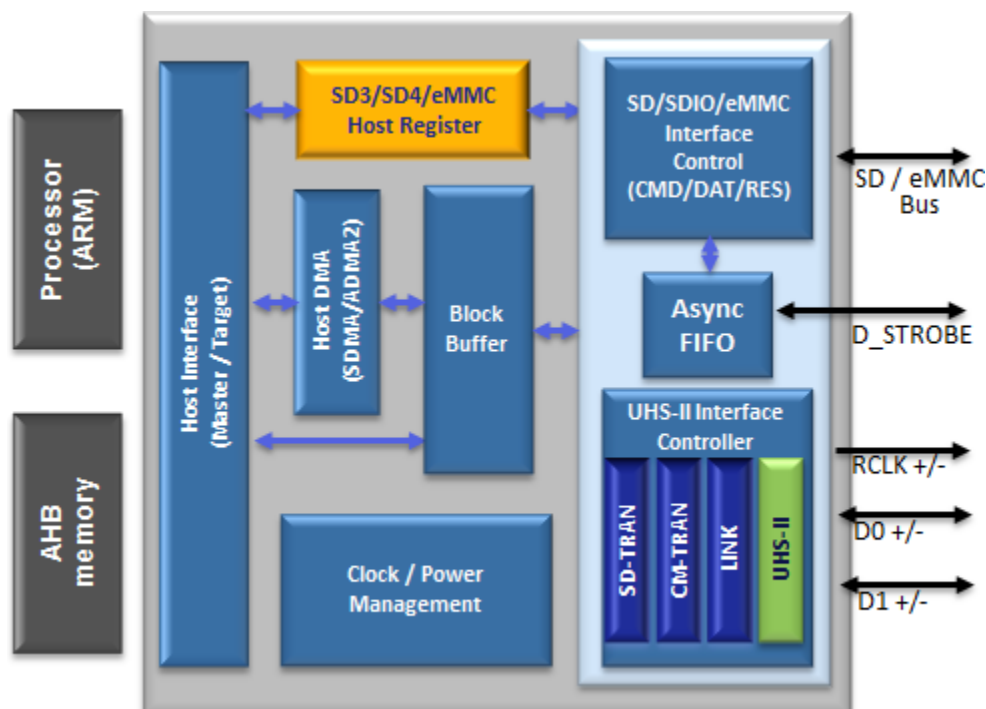


Figure 1 - eMMC5.1/SD3.0/SDIO3.0 Host Controller Functional Block Diagram

2.2 Features

- Compliant with the following specifications:
 - JEDEC eMMC Specification Version 5.1
 - JEDEC eMMC CQHCI (part of eMMC5.1)
 - SDA Part A2 SD Host Controller Version 3.00
 - SDA Part 1 Physical Layer Specification Version 3.00
 - SDA Part E1 SDIO Specification Version 3.00
 - AMBA, AHB Specification Version 2.00
 - AMBA, Advanced Extensible Interface (AXI) Specification Version 1.00 (Optional)
 - Open Core Protocol (OCP) Specification Version 2.2 (Optional)
- The core supports:
 - 32-bit and 64-bit system data bus.
 - 32-bit and 64-bit system addressing.
 - Interrupts and wake up functionality
 - Internal Clock divider for various card operational modes
 - One of the AHB, AXI or OCP System/Host bus
- The data is transferred using:
 - Programmed Input/Output (PIO) mode on the Host Bus Slave interface
 - Direct Memory Access (DMA) mode using Simple DMA (SDMA) or Advanced DMA (ADMA2) on the Host Bus Master interface*
 - Configurable FIFO size to support different block sizes.

Note: The Host Bus is AHB or AXI or OCP.

- eMMC 5.1 features:
 - HS400 high speed interface timing mode of up to 400 MB/s data rate
 - Transfers the data in HS400, HS200, DDR52 modes.
 - 4KB block support
 - Tuning for HS200 mode
 - Command Queuing for High Performance data transfers with Hardware Acceleration.
 - Enhanced strobe function for reliable operation at HS400 mode.
 - MMC Plus and MMC Mobile
 - Host clock rate variable between 0 and 200 MHz
 - Transfers the data in 1-bit, 4-bit and 8-bit modes
 - Supports legacy modes (Default Speed, High Speed).
 - CRC7 for command and CRC16 for data integrity
 - Password protection of cards

- UHS-I features (SD3.0/SDIO3.0):
 - 1.8V voltages switch operation
 - Tuning for SDR104 mode
 - Host clock rate variable between 0 and 208 MHz
 - Up to 832 Mbps data rate using 4 parallel data lines (SDR104 mode)
 - Transfers the data in 1-bit and 4-bit SD modes.
 - Transfers the data in SDR104, DDR50, SDR50, SDR25, SDR12, DS and HS modes
 - Cyclic Redundancy Check (CRC): CRC7 for commands, CRC16 for data integrity
 - Variable-length data transfers
 - Performs Read Wait Control, Suspend/Resume operation with SDIO CARD
 - Designed to work with I/O cards, Read-only cards and Read/Write cards
 - Card Detection (Insertion/Removal)
 -

2.3 IP Deliverables for RTL Version

- Verilog HDL of the IP Core
- Synthesis scripts
- Test environment and test scripts
- User guide