



Silicon Dreams
S I L I C O N T O T H E P O W E R O F Y O U R D R E A M S

eMMC 5.1 Device Controller IP

Datasheet

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1 Introduction

Silicon Dreams is a provider of licensable Intellectual Property Cores for the Semiconductor industry along with software development and SoC design services.

Silicon Dreams was founded in 2022 to address the burgeoning semiconductor industry and its timing was well founded with the company's explosive growth along with the AI boom. The company is rapidly expanding its operations internationally to be closer to its customer base.

We have licensees Worldwide with most of our customers based in the USA followed by the APAC region with a significant presence in China and Japan.

Our goal is to enable customers to realize their dreams on silicon through our licensable intellectual property cores, design services and software.

The company can also build custom silicon per the customers specifications.

2 eMMC 5.1 Device Controller Datasheet

2.1 Overview

eMMC 5.1 (JEDEC Item # JC-64.1-67.14) is the latest specification defined by JEDEC and is designed to meet the requirements for next level of high performance data transfer for mobile electronic products. With its low-pin count, higher bandwidth, multiple boot mechanisms, and content security features, eMMC 5.1 provides an easy migration path and greatly simplifies system design for new products.

Silicon Dreams's eMMC 5.1 Device Controller IP is compliant to the latest eMMC specification. The controller provides a bandwidth of up to 3.2 Gbps (400 MB/s) in HS400 DDR mode running with 200MHz clock. A NAND Flash controller can be connected to the eMMC controller. In such an implementation, the controller's AHB interface provides a channel for data transfers between the eMMC device controller and a NAND flash controller which is also available from Silicon Dreams.

The eMMC device IP supports all new features. The eMMC device IP is backward compatible to previous versions of eMMC, including HS400, HS200, MMC 1-bit, 4-bit, and 8-bit modes.

eMMC device IP simplifies system design by supporting power-on booting without the upper level of software driver. The eMMC controller shields the host system from the functional differences among various NAND flash architectures such as MLC. The explicit sleep mode allows the host system to instruct the eMMC device controller to directly enter a low power sleep mode. The controller supports block lengths or sector sizes of 512, 1024, 2048 and 4096 bytes.

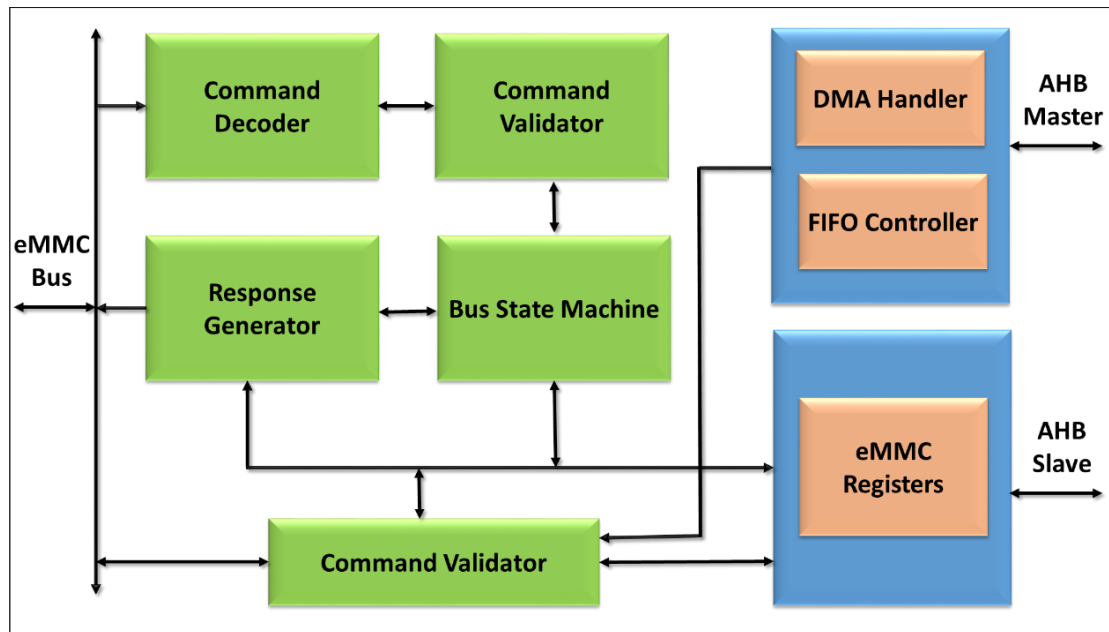


Figure - Device Controller Functional Block Diagram

2.2 Features

- eMMC 5.1 Features
 - Supports Command Queuing
 - Supports Enhanced Strobe in HS400 Mode
 - Supports Cache Barrier
 - Supports Added Cache Flushing report
 - Supports RPMB Throughput Improve.
 - Supports write data size 8KB (thirty two 512B frames)
 - Supports Background Operation Control
 - Supports Secure Write Protection
- eMMC 5.0 Features:
 - Supports HS400 high speed interface timing mode up to 400MB/s data rate
 - Supports field firmware update
 - Supports eMMC device health report
 - Supports eMMC production state awareness
 - Supports secure removal types
 - Supports sleep notification
- eMMC 4.51 Features:
 - Complies with JESD84-B451 Embedded Multimedia Card, Electrical Standard (4.51 Device)
 - Supports high speed interface timing mode of up to 200 MB/s single data rate bus (HS200)

- Supports tuning concept for read operation
 - Supports DDR interface with data transfer rate of 104 MB/s
 - Supports new H/W Reset pin
 - Supports Power-On Write Protection groups, Temporary and Permanent Write Protection features
 - Supports Alternative Boot operation mode
 - Supports Write Protection features on H/W Reset
 - Supports Replay Protected Memory Block (RPMB) and access control
 - Supports partition management by defining general purpose partition with enhancement attribute features
 - Supports Write Protection on Boot area
 - Supports Boot operation in High Speed and DDR mode
 - Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity
 - Full backward compatibility with previous multimedia card systems (1-bit data bus, multi card systems)
 - Supports general purpose R/W command
 - Size of eMMC device capacity can be more than 2GB
 - Supports block lengths of 512 bytes and sector size of 4K bytes for high capacity
 - Error injection capabilities
 - Supports Boot operation mode in simple boot sequence method
 - Supports Sleep mode for power saving
 - Supports Reliable Write operation that performs safe-updates on sudden power failure
 - Supports Packed command flow sequence
 - Supports Power-Off notification flow
 - Supports Discard and Sanitize command
 - Supports context IDs and data tag mechanism
 - Supports security protocol write and read command
 - Supports secure erase and secure trim
- AMBA Compliance:
 - Complies with AMBA specification version 2.0
 - Supports Incremental Burst Transfers on DMA mode
 - Supports Register Transfer on non DMA mode
 - Supports Retry and Split
- Speed Classes Supported:
 - Silicon Dream's IP supports MMC speed classes: 0, 2, 4, 5, 6, 7, 8, 9, 10.
- Card Enumeration:
 - The eMMC Device IP is enumerated by a host. Card insertion or removal in the slot is signaled to the host. The type of the card and supported memory size are informed to the host controller via CID, CSD, Ext_CSD registers housed inside the eMMC Device IP.

2.3 IP Deliverables

- Verilog HDL
- Synthesis scripts
- Test Environment and test scripts
- User Guide