



Silicon Dreams
SILICON TO THE POWER OF YOUR DREAMS

I3C Host Controller IP

Datasheet

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1 Introduction

Silicon Dreams is a provider of licensable Intellectual Property Cores for the Semiconductor industry along with software development and SoC design services.

Silicon Dreams was founded in 2022 to address the burgeoning semiconductor industry and its timing was well founded with the company's explosive growth along with the AI boom. The company is rapidly expanding its operations internationally to be closer to its customer base.

We have licensees Worldwide with most of our customers based in the USA followed by the APAC region with a significant presence in China and Japan.

Our goal is to enable customers to realize their dreams on silicon through our licensable intellectual property cores, design services and software.

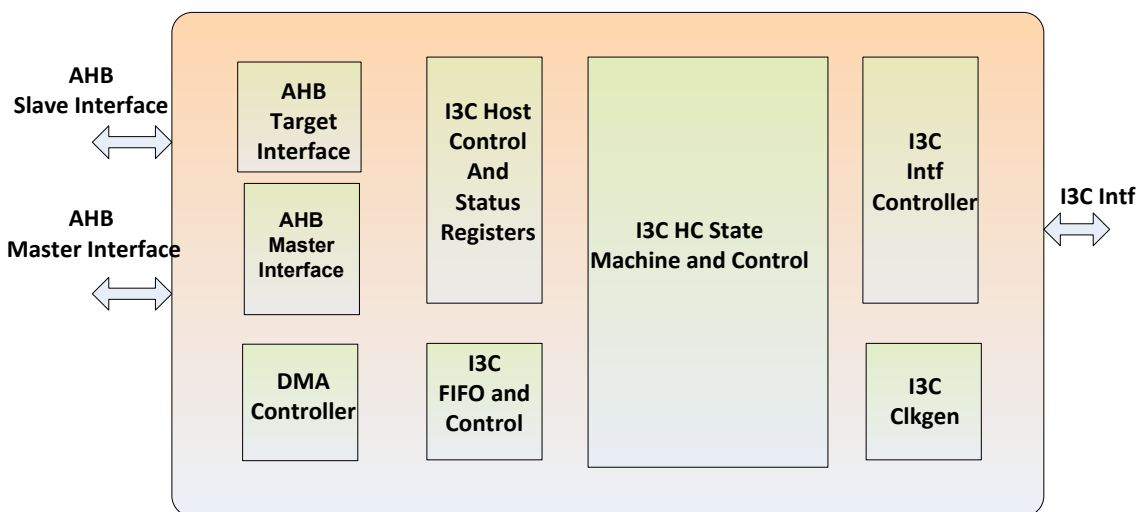
The company can also build custom silicon per the customers specifications.

2 I3C Host Controller IP

2.1 Overview

The Silicon Dreams I3C Host Controller IP implements Host Controller functionality as defined by the MIPI Alliance's I3C Specification. The I3C bus is used for various sensors in the mobile/automotive system where the Host Controller transfers data and control between itself and various sensor devices. The I3C Host Controller IP Core provides a 32-bit AHB bus as the application interface to configure and control the I3C Host Controller IP Core. The I3C Host Controller IP can be easily integrated into an SOC to provide the required I3C functionality. Also, the I3C Host Controller IP provides direct signaling to connect to the IO Buffers (SCL and SDA). Please note that the user needs to provide appropriate IO buffers to meet the I3C specification.

The I3C Host Controller implements support for legacy I2C Device Controllers, Clock frequency scaling, Open-drain and Push-pull operation of I3C Interface, and Dynamic Addressing support. The I3C Host Controller supports the required SDR mode with Clock frequency of up to 12.5 MHz and also the HDR modes as defined by the I3C Specification. The included FIFO (Configurable) is used to handle data transfers between IP and the external Device Controllers.



I3C Host Controller Block Diagram

2.2 Features

- Compliant with MIPI I3C Specification v1.2
- Compliant with MIPI I3C HCI Specification v1.1
- Supports up to 12.5 MHz operation using Push-Pull
- Supported features,
 - Open-Drain and Push-pull type transactions (as required)

- Supports legacy I2C devices
- Dynamic addressing while supporting Static addressing for Legacy I2C devices
- Legacy I2C messaging
- I2C-like Single Data Rate messaging (SDR)
- High Data Rate messaging modes (HDR-DDR, HDR-TSP, HDR-TSL modes)
- Reception of In-band Interrupt support from the I3C Device Controllers
- Reception of Hot-Join from newly added I3C Device Controllers
- Support for Target reset
- Support for group addressing
- AHB Target Interface for Configuring/Controlling the IP with Interrupt output
- AHB Interface for Host Controller DMA access
- Support for up-to Eight rings in DMA mode and configurable as per the application requirement
- Support for JESD403-1 Sideband Interface
- Configurable FIFO sizes for PIO, DMA, Command, Response, and IBI Queue. Common FIFOs are used for both PIO and DMA modes.

2.3 Deliverables

- RMM compliant synthesizable RTL design in Verilog
- Easy-to-use Test environment
- Synthesis scripts
- Technical documents
- Validated with 3rd Party Device Controller VIP and available as an additional option