



Silicon Dreams
SILICON TO THE POWER OF YOUR DREAMS

I3C Device Controller IP

Datasheet

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1 Introduction

Silicon Dreams is a provider of licensable Intellectual Property Cores for the Semiconductor industry along with software development and SoC design services.

Silicon Dreams was founded in 2022 to address the burgeoning semiconductor industry and its timing was well founded with the company's explosive growth along with the AI boom. The company is rapidly expanding its operations internationally to be closer to its customer base.

We have licensees Worldwide with most of our customers based in the USA followed by the APAC region with a significant presence in China and Japan.

Our goal is to enable customers to realize their dreams on silicon through our licensable intellectual property cores, design services and software.

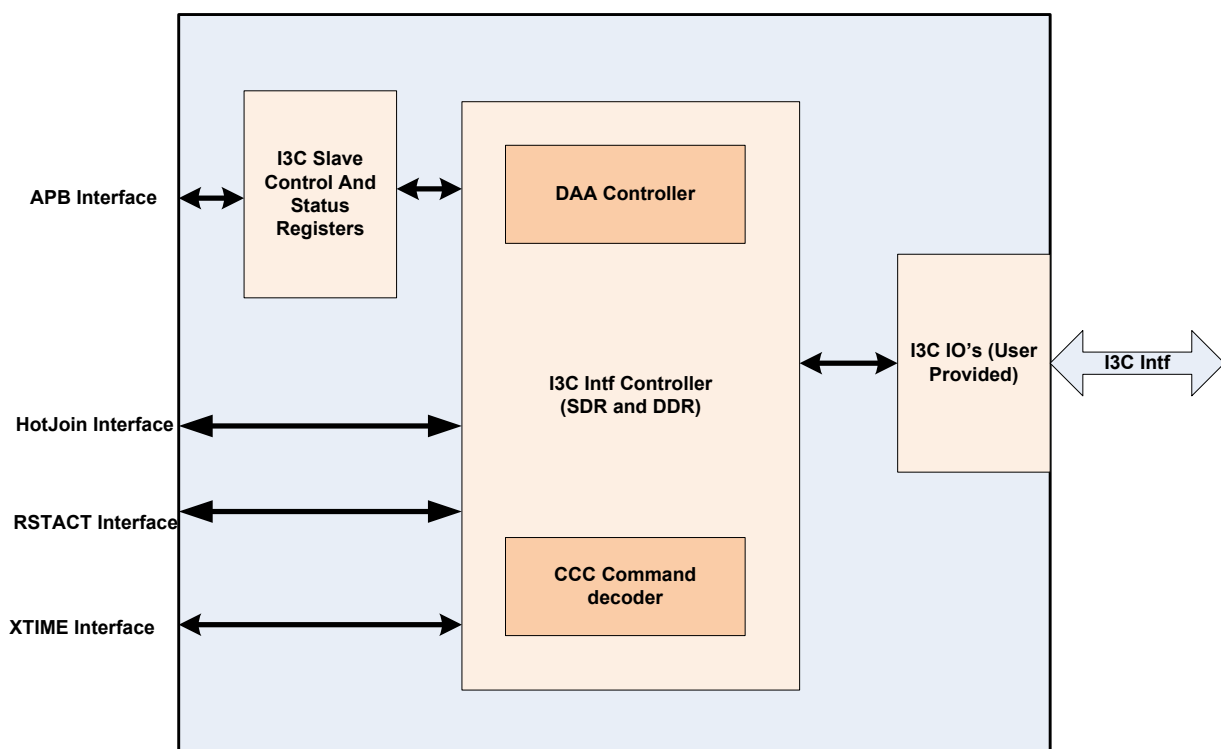
The company can also build custom silicon per the customers specifications.

2 I3C Device Controller IP with APB Interface

2.1 Overview

The Silicon Dreams I3C Device Controller IP Implements Device Controller functionality as defined by the MIPI Alliance's I3C Specification. The I3C bus is used for various sensors in the mobile/automotive system where an I3C Host Controller transfers data and control information between itself and various sensor devices. The I3C Device Controller IP can be easily integrated into the Sensor/Device Controllers with minimal gate count.

The I3C Device Controller is highly configurable (synthesis time) to provide an optimal solution based on the Device's requirements. This includes, acting as a legacy I2C device, Support for Dynamic Address Assignment, HDR, and a configurable FIFO for data transfers. In addition, Optional I3C Device Controller functions like Interrupt generation, Hot-Join request generation. The I3C Device Controller IP provides direct signaling to connect to the IO Buffers (SCL and SDA). Please note that the user needs to provide appropriate IO buffers to meet the I3C specification.



I3C Device Controller with APB Interface Block Diagram

2.2 Features

- Compliant with MIPI I3C Specification v1.2

- Supports up to 12.5 MHz operation using Push-Pull
- Open-Drain and Push-pull type transactions (as required)
- Acts as a legacy I2C Device Controller while supporting legacy I2C Messaging and protocol
- Supported features,
 - Dynamic address assignment
 - Address arbitration
 - In-band Interrupt
 - Hot Join request handling
 - HDR Capable – HDR-DDR, HDR-TSP, HDR-TSL modes
 - CCC Command features
 - Private read and write transfers
 - Data transfer with and without broadcast
 - Legacy I2C support
 - Timing Control
 - Group addressing
 - Target reset handling
 - JESD403-1 Sideband interface
- APB Target Interface for Configuring and Controlling the IP with interrupt and for data transfers, IBI

2.3 Deliverables

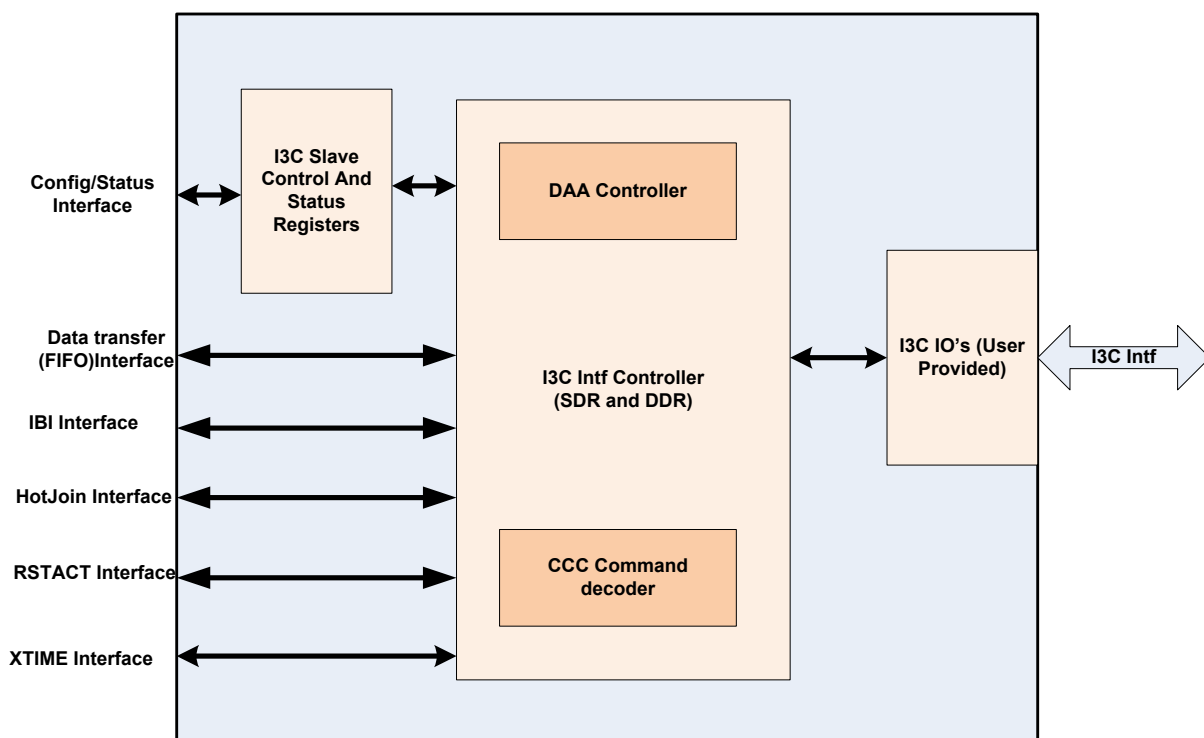
- RMM compliant synthesizable RTL design in Verilog
- Easy-to-use Test environment
- Synthesis scripts
- Technical documents
- Validated with 3rd Party Host Controller VIP and available as an additional option

3 I3C Device Controller IP with FIFO Interface

3.1 Overview

The Silicon Dreams I3C Device Controller IP Implements Device Controller functionality as defined by the MIPI Alliance's I3C Specification. The I3C bus is used for various sensors in the mobile/automotive system where an I3C Host Controller transfers data and control information between itself and various sensor devices. The I3C Device Controller IP can be easily integrated into the Sensor/Device Controllers with minimal gate count.

The I3C Device controller is highly configurable (synthesis time) to provide an optimal solution based on the Device's requirements. This includes acting as a legacy I2C device, Support for Dynamic Address Assignment, DDR. In addition, optional I3C Device functions like Interrupt generation, and Hot-Join request generation. The I3C Device Controller also supports both Synchronous and Asynchronous Time stamping functions by providing support for SETXTIME/GETXTIME commands. Also, the I3C Device Controller IP provides direct signaling to connect to the IO Buffers (SCL and SDA). **Please note that the User needs to provide appropriate IO buffers to meet the I3C specification.**



I3C Device Controller with FIFO Interface IP Block Diagram

3.2 Features

- ❖ Compliant with MIPI I3C Specification v1.2
- ❖ Supports up to 12.5 MHz operation using Push-Pull
- ❖ Standard Feature Includes
 - Dynamic address assignment
 - Group addressing
 - Address arbitration
 - In-band Interrupt handling
 - Hot Join request handling
 - SDR and HDR(HDR-DDR) capable
 - CCC Command features
 - Private Read and Write transfers
 - Legacy I2C support
 - Timing Control through XTIME Interface
 - Target reset handling
- ❖ Side Band interface to transfer CCC commands, Read, Write transfer
- ❖ Side Band interface for In-band and hot join handling

3.3 Deliverables

- RMM compliant synthesizable RTL design in Verilog
- Easy-to-use Test environment
- Synthesis scripts
- Technical documents
- Validated with 3rd Party Host Controller VIP and available as an additional option