



Silicon Dreams
S I L I C O N T O T H E P O W E R O F Y O U R D R E A M S

DSI-2 Tx and Rx IP

Datasheet

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1 Introduction

Silicon Dreams is a provider of licensable Intellectual Property Cores for the Semiconductor industry along with software development and SoC design services.

Silicon Dreams was founded in 2022 to address the burgeoning semiconductor industry and its timing was well founded with the company's explosive growth along with the AI boom. The company is rapidly expanding its operations internationally to be closer to its customer base.

We have licensees Worldwide with most of our customers based in the USA followed by the APAC region with a significant presence in China and Japan.

Our goal is to enable customers to realize their dreams on silicon through our licensable intellectual property cores, design services and software.

The company can also build custom silicon per the customers specifications.

2 DSI-2 IP

2.1 Overview

Silicon Dreams is a leading SOC IP provider of a complete suite of MIPI compliant IP solutions, which consist of IP cores, verification IP, software stacks and drivers, protocol analyzers, hardware platforms for software development and compliance testing, and optional customization services. The MIPI compliant IP cores are interface building blocks that simplify interconnect architectures in mobile platforms. This leads to smaller footprint, greater interoperability between mobile IP, chips and devices from diverse sources, and lower power and EMI.

This document describes the Silicon Dreams IP Core that functions as a MIPI DSI Host Controller, which typically resides in a mobile platform's application processor, and communicates over a D/C-PHY serial link to a DSI Device in the display panel.

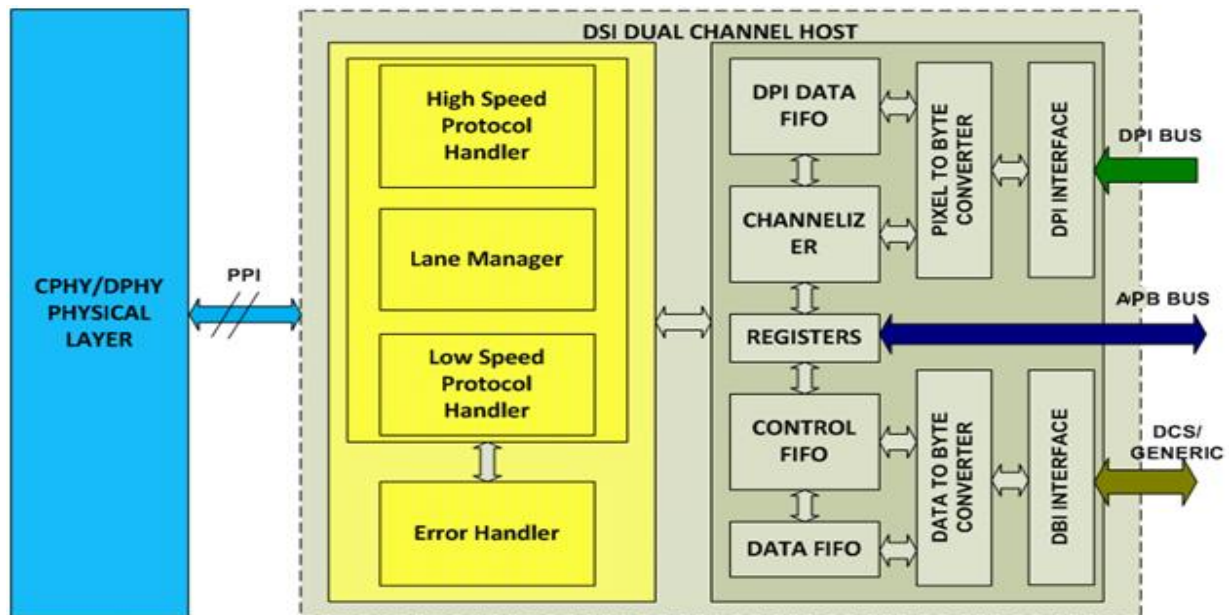


Figure: DSI-2 Tx Block Diagram

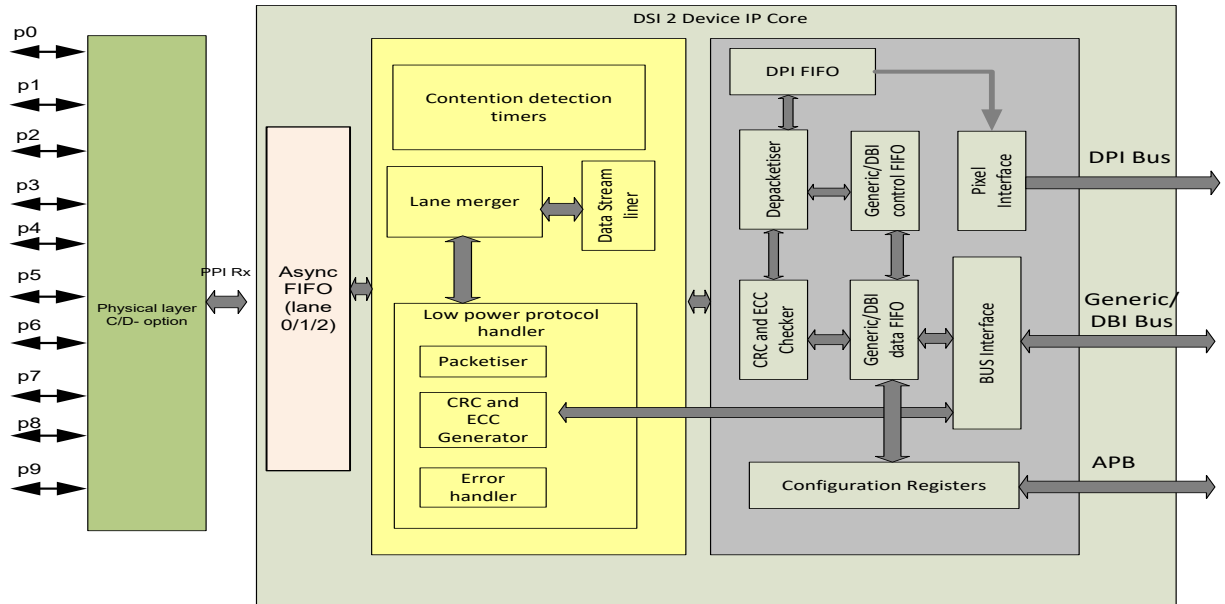


Figure: DSI-2 Rx Block Diagram

2.2 DSI-2 Features

- Compliant with the following MIPI specifications:
 - Display Serial Interface (DSI 2) version 1.1
 - Display Pixel Interface (DPI-2) version 2.00
 - Display Bus Interface (DBI) version 2.00
 - Display Command Set (DCS) version 1.3
 - D-PHY version 1.2
 - C-PHY version 1.1
- DSI Host-side (display module) interface supports:
 - Connectivity to D-PHY / C-PHY through PPI Interface
 - 1 to 4 data lane for DPHY mode and 1 to 3 data lane for CPHY mode
 - Hi-Speed (HS) transmit from 80 Mbps to 1.5Gbps per lane without deskew calibration
 - Hi-Speed (HS) transmit from 1.5Gbps < 2.5 Gbps per lane with deskew calibration
 - Low Power (LP) receive/transmit from/to device at 10 Mbps
 - Continuous and stoppable clocks on clock lane
 - Bus turnaround with contention and fault recovery
 - Switching to and from Low Power (LP) and Ultra-low Power (ULPS) modes
 - EOT enable/disable mechanisms
 - Multiple packets per transmission with interleaved data stream
 - Programmable error injection in Verification IP and error detection in design IP
 - Flexibility in setting polarity for DPI Interface signals
- Application Processor Connectivity and Video Command Processing
 - DPI or DBI, depending on panel or display unit architecture
 - Generic command support
 - Generic parallel interface for sending and receiving vendor-specific information to and from the display driver logic in the display module
 - Support for all generic read/writes over DBI/Generic interface
- Video Mode supports:
 - Wide range of display resolution and pixel formats
 - Display resolutions: QQVGA, QCIF, QVGA, CIF, VGA, WVGA, XGA, 1080p, QXGA, QSXGA
 - Burst mode and non-burst transfers over DPI interface
- DBI supports:
 - 8/9/16-bit data transfer in DBI Type B interface
 - All DCS commands
- AHB/APB Interface for register configuration and monitoring using programmed IO

2.3 Deliverables

- Verilog HDL of the IP core
- Unencrypted test bench environment
- Synthesis scripts
- Lint report
- CDC report
- Gate count estimation available upon request
- Technical documentation
 - IP user guide
 - Simulation user guide