



Silicon Dreams
S I L I C O N T O T H E P O W E R O F Y O U R D R E A M S

MIPI DPHY IP

Datasheet

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1 Introduction

Silicon Dreams is a provider of licensable Intellectual Property Cores for the Semiconductor industry along with software development and SoC design services.

Silicon Dreams was founded in 2022 to address the burgeoning semiconductor industry and its timing was well founded with the company's explosive growth along with the AI boom. The company is rapidly expanding its operations internationally to be closer to its customer base.

We have licensees Worldwide with most of our customers based in the USA followed by the APAC region with a significant presence in China and Japan.

Our goal is to enable customers to realize their dreams on silicon through our licensable intellectual property cores, design services and software.

The company can also build custom silicon per the customers specifications.

2 D-PHY1.1 (1.5Gbps)

2.1 Overview

The DPHY is a semiconductor chip with Universal DPHY functionality that can interface with Camera and Display interfaces, both transmit and receive, and capable of meeting line rates of 1.5Gbps/lane. This product offers complete debug facilities to validate Application processors with MIPI interfaces, MIPI Cameras and MIPI displays.

In Silicon Dreams D-PHY digital IP, both Master and slave modes have state machines to generate sequences for switching to high speed, control mode and ultra low power modes. They have de-serializer / serializer unit to convert parallel to serial data and vice-versa. Slave device has sequence observer state machines to know the modes of operation of the lanes. They have sequence error detectors also.

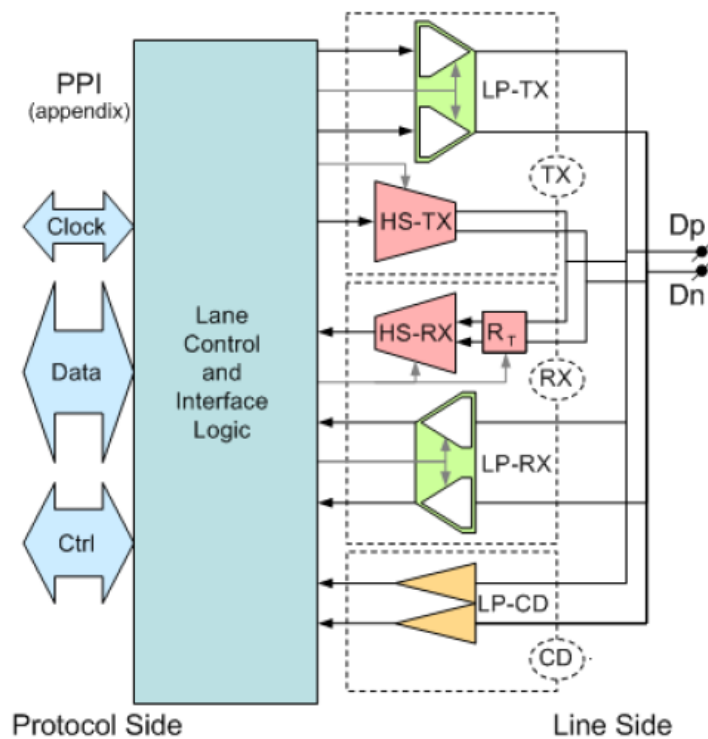


Figure : Block diagram of DPHY

2.2 Features

- Complaint to MIPI Alliance Standard for D-PHY specification Version 1.1
- Supports synchronous transfer at high speed mode with a bit rate of 80-1500 Mb/s
- Supports asynchronous transfer at low power mode with a bit rate of 10 Mb/s
- Spaced one hot encoding for Low power [LP] data
- One byte buffer is housed inside the core for both data-out and data-in paths.
- Supports one clock lane and two data lanes.
- Supports error detection mechanism for sequence errors and contentions
- Data lanes support transfer of data in high speed mode.
- Supports ultra low power mode, high speed mode and control mode.
- Has clock divider unit to generate clock for parallel data reception and transmission from and to the PPI
- Activates and disconnects high speed terminators for reception and transmission.
- Supports standard PHY transceiver compliant to MIPI Specification
- Supports standard PPI interface compliant to MIPI Specification.
- Clock lane supports unidirectional communication
- On-chip clock generation configurable for either transmitter or a receiver
- Testability for Tx, Rx and PLL
- PHY can be configured as a master or slave.
- Core is structured to increase the number of data lanes .
- Supports High speed mode in Forward communication
- Support for Stuck-At scan
- Includes A-BIST for high-speed loopback testing

2.3 Deliverables

- GDS-II
- CDL netlist for LVS
- LVS reports
- DRC and Antenna reports
- LIB files
- User guide and Integration Guides
- LEF
- Scan-inserted netlist for DFT
- Verification Environment with behavioral models
- IBIS Models

3 D-PHY1.2 (2.5Gbps)

3.1 Overview

The ever increasing demand for band width for the high resolution cameras resulted into search for a simple, cost effective, rate efficient PHY which can support high data rate. This search resulted into a new kind of PHY, which even at less channel rate provides high data rate.

Silicon Dream's DPHY1.2 IP can achieve high data rate of 2.5Gbps per lane. DPHY reuses the similar Low power signaling.

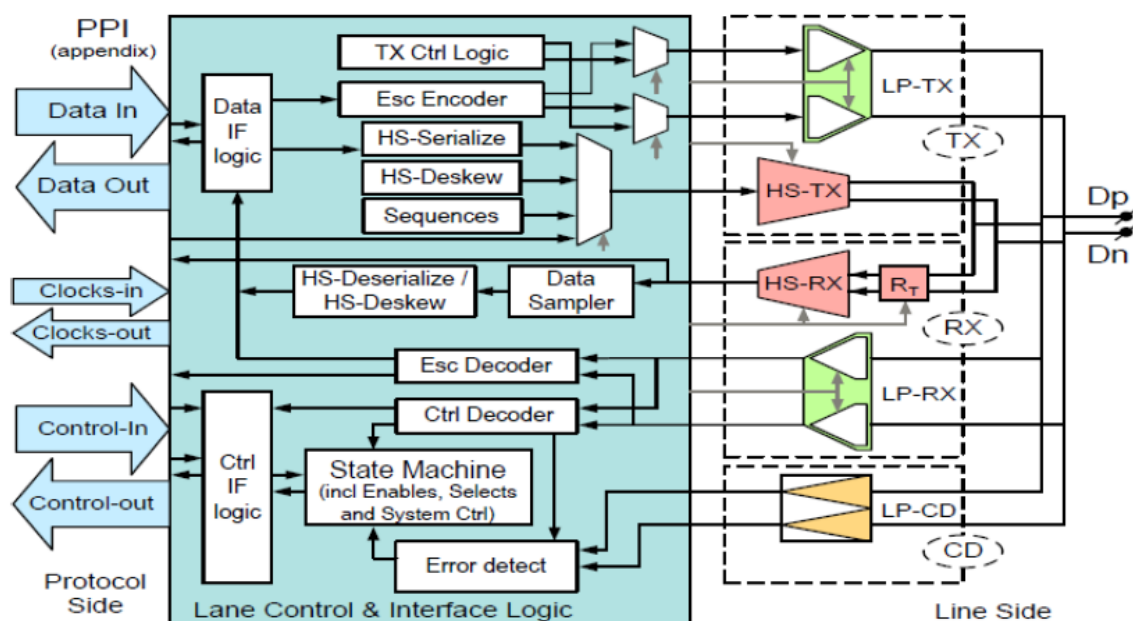


Figure : DPHY Lane Architecture

3.2 Features

- Compliant to DPHY 1.2 specification
- Supports DSI2-1.1
- Supports synchronous transfer at high speed mode with a bit rate of 40-2500Mbps for DPHY1.2
- Supports up to one clock lane and four data lanes for DPHY1.2
- Deskew support for the DPHY 1.2
- Supports error detection mechanism for sequence errors and contentions
- Supports ultra-low power mode, high speed mode and control mode.

- Has clock divider unit to generate clock for parallel data reception and transmission from and to the PPI
- Activates and disconnects high speed terminators for reception and transmission.
- Supports standard PHY transceiver compliant to MIPI Specification
- Supports standard PPI interface compliant to MIPI Specification DPHY1.2
- Clock lane supports unidirectional communication
- On-chip clock generation configurable for either transmitter or loopback (BIST)
- PHY can be configured as a master or slave.
- Testability for Tx, Rx and PLL
- Built in Self Test for DPHY
- Core is structured to increase the number of data lanes
- Supports scan insertion and stitching for DFT
- Supports additional flexibility in terms of data lane/line polarity swapping
- Provides extensive debug capability and access which facilitate easy silicon debug and device characterization

3.3 Deliverables

- GDS-II
- CDL netlist for LVS
- LVS reports
- DRC and Antenna reports
- LIB files
- User guide and Integration Guides
- LEF
- Scan-inserted netlist for DFT
- Verification Environment with behavioral models
- IBIS Models

4 D-PHY2.5 (4.5Gbps)

4.1 Overview

The DPHY is a semiconductor chip with Universal DPHY functionality that can interface with Camera and Display interfaces, both transmit and receive, and capable of meeting line rates of 4.5Gbps/lane. This product offers complete debug facilities to validate Application processors with MIPI interfaces, MIPI Cameras and MIPI displays.

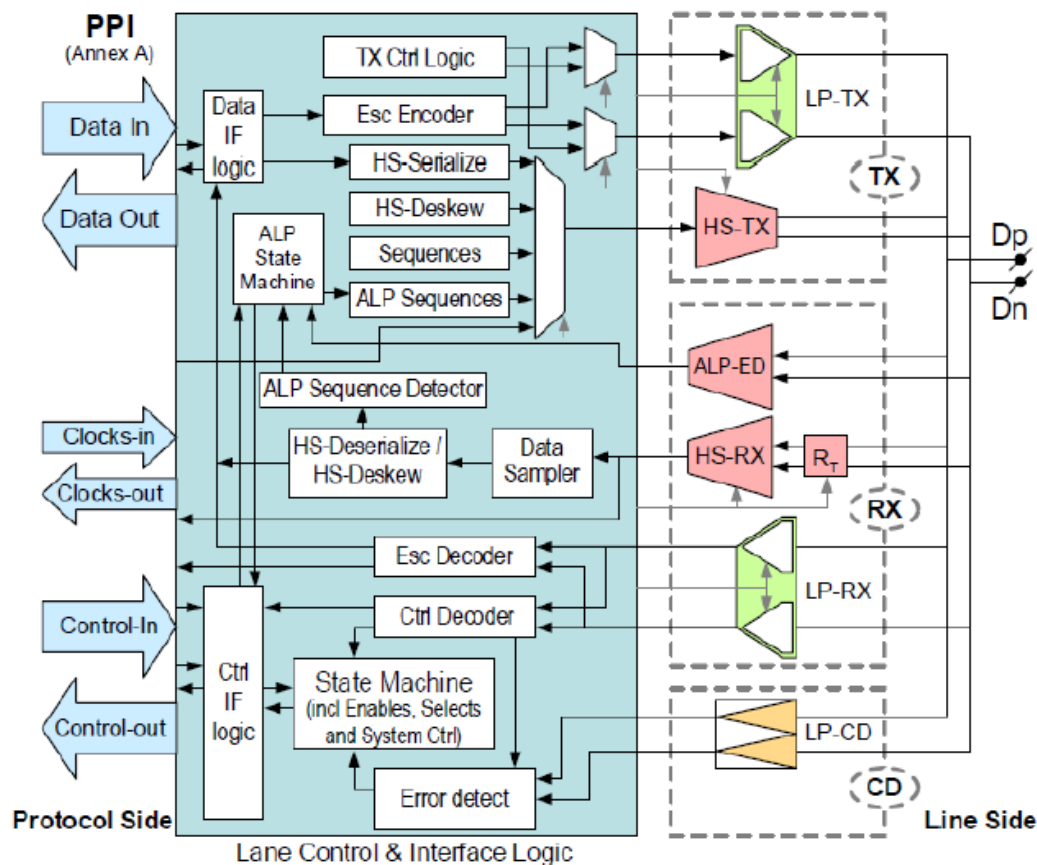


Figure : DPHY Lane Architecture

4.2 Features

- Compliant with MIPI Alliance Standard for D-PHY specification Version 2.5
- Supports synchronous transfer at high speed mode with a bit rate of 80-1500 Mb/s without deskew calibration, up to 2500 Mb/s with deskew calibration and up to 4500 Mb/s with equalization
- Supports Spread Spectrum Clocking

- Supports asynchronous transfer at low power mode with a bit rate of 10 Mb/s
- Spaced one hot encoding for Low power [LP] data
- Supports one clock lane and four data lanes
- Supports error detection mechanism for sequence errors and contentions on Data lanes
- Supports transfer of data in high-speed mode
- Supports ultra-low power mode, alternate low power, high-speed mode and LP control mode.
- Register controls to connect and disconnect high-speed terminators inside the Analog for reception and transmission
- Supports standard PPI interface compliant with MIPI Specification
- Clock lane supports unidirectional communication
- PHY can be configured as a master or slave
- Supports "HS deskew" and "Alternate Calibration Sequence"
- Support for "Preamble sequence"
- Supports High speed reverse communication and fast lane turnaround
- Support for polarity swap for all lanes between Dp/Dn
- APB register access to all DPHY registers
- Supports SCAN and BIST modes
- Support for BIST methodology as per the DPHY standard specification Verion 2.5

4.3 Deliverables

- GDS-II
- CDL netlist for LVS
- LVS reports
- DRC and Antenna reports
- LIB files
- User guide and Integration Guides
- LEF
- Scan-inserted netlist for DFT
- Verification Environment with behavioral models
- IBIS Models