



Silicon Dreams
S I L I C O N T O T H E P O W E R O F Y O U R D R E A M S

CSI-2 v2.1 Transmitter IP

Datasheet

Silicon Dreams Private Limited
Regd.office: C-103, Sipcot Complex,
Sinnamani Nagar II, Bye Pass Road,
Thoothukudi -628008
TamilNadu, India

Ph : 0461-2363334

1. Introduction

Silicon Dreams is a provider of licenseable Intellectual Property Cores for the Semiconductor industry along with software development and SoC design services.

Silicon Dreams was founded in 2022 to address the burgeoning semiconductor industry and its timing was well founded with the company's explosive growth along with the AI boom. The company is rapidly expanding its operations internationally to be closer to its customer base.

We have licensees Worldwide with most of our customers based in the USA followed by the APAC region with a significant presence in China and Japan.

Our goal is to enable customers to realize their dreams on silicon through our licenseable intellectual property cores, design services and software.

The company can also build custom silicon per the customers specifications.

2. CSI-2 v2.1 Transmitter IP

2.1 Overview

Silicon Dreams is a leading SOC IP provider of a complete suite of MIPI compliant IP solutions, which consist of IP cores, verification IP, software stacks and drivers, protocol analyzers, hardware platforms for software development and compliance testing, and optional customization services.

The MIPI compliant IP cores are interface building blocks that simplify interconnect architectures in mobile platforms. This leads to smaller footprint, greater interoperability between mobile IP, chips and devices from diverse sources, and lower power and EMI.

This document describes the Silicon Dreams IP Core that functions as a MIPI CSI-2 Transmitter, which typically resides in a mobile platform's camera module, and communicates over a D-PHY/C-PHY link to a CSI2 Receiver in the applications processor. The Silicon Dreams CSI-2 combo IP is MIPI-compliant and provides a standard, scalable, low-power, high-speed interface that supports a wide range of higher image resolutions.

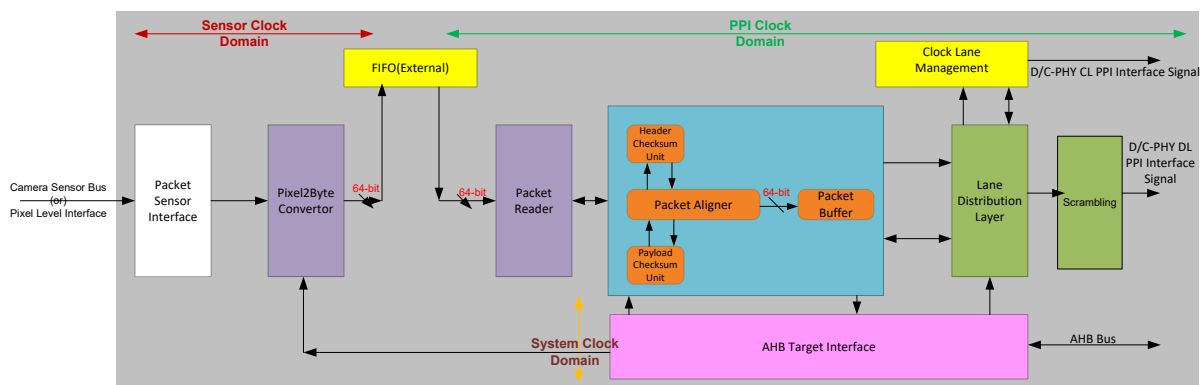


Figure 3 Combo Transmitter Functional Block Diagram

2.2 Features

- Compliant with the following MIPI specifications:
 - CSI2 specification v2-1
 - DPHY specification v2-1
 - DPHY specification v1-2
 - CPHY specification v1-2

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- CSI-2 Combo Transmitter Core features:
 - Use of either D-PHY/C-PHY by user configuration
 - Lane Configurability depending on the bandwidth requirements of the application, up to 8-lanes for DPHY and up to 3-lanes for C-PHY
 - Connectivity to DPHY/CPHY through MIPI PPI Interface
 - High Speed (HS) receiver rates of 182Mbps (80Msps) to 6840Mbps (3Gsps) per lane with C-PHY interface
 - High Speed (HS) receiver rates of 80Mbps to 1500Mbps per lane without calibration, 1500Mbps to 2500 Mbps with skew calibration and 2500Mbps to 4500Mbps with equalization in D-PHY interface
 - Supports for Alternate Low Power State (ALPS) in CPHY mode
 - Support for Ultra Low Power Mode (ULPS)
 - Support for Continuous and Non-Continuous Clock Mode
 - Pixel formats supported
 - RAW data type
 - YUV data type
 - RGB data type
 - All user Defined data types / JPEG
 - Generic 8-bit long packet data types
 - Supports Data Type Interleaving
 - Supports Virtual Channel Interleaving
 - Supports Virtual Channel extension as 16 VCs in DPHY mode and 32 VC's in CPHY mode
 - Support for optional feature Data scrambling
 - Support for CPHY lane deskew
 - Support for Packet spacing LRTE/EPD feature (optional)
 - Pixel Level Input Interface for Image Sensor
 - Supports Header and Payload Checksum
 - Configurable for two mode of operation
 - Store and Forward Mode – Stores the full pixel packet before forwarding.
 - Cut through Mode – Initiates the HS transmission to D/CPHY as soon as the pixel information is received. Makes use of very shallow memory.
 - Supports Multi Pixel Mode – Multiple Pixels per clock to bring down the sensor clock frequency to support higher resolution applications
 - PPI Data Lane swapping as per user configuration
 - Optional support for Compressed data formats
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- Host interface for register configuration and monitoring,
 - Used for programming both CSI-2 and PHY related registers. Reserved address space [0x00 – 0x0F] for the PHY related registers.
 - Optional support for the AHB/APB Interface

2.3 IP Deliverables

- Verilog HDL of the IP core
- User guide
- Synthesis scripts
- Lint report
- CDC report
- Verilog test suite
- Gate count estimation available upon request