



Silicon Dreams
S I L I C O N T O T H E P O W E R O F Y O U R D R E A M S

CSI-2 v1.3 Receiver IP

Datasheet

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1. Introduction

Silicon Dreams is a provider of licensable Intellectual Property Cores for the Semiconductor industry along with software development and SoC design services.

Silicon Dreams was founded in 2022 to address the burgeoning semiconductor industry and its timing was well founded with the company's explosive growth along with the AI boom. The company is rapidly expanding its operations internationally to be closer to its customer base.

We have licensees Worldwide with most of our customers based in the USA followed by the APAC region with a significant presence in China and Japan.

Our goal is to enable customers to realize their dreams on silicon through our licensable intellectual property cores, design services and software.

The company can also build custom silicon per the customers specifications.

2. CSI-2 v1.3 Receiver IP

2.1 Overview

Silicon Dreams is a leading System on Chip (SoC) Intellectual Property (IP) provider of a complete suite of Mobile Industry Processor Interface (MIPI) compliant IP solutions, which consists of IP cores, verification IP, software stacks and drivers, protocol analyzers, hardware platforms (HVP's) for software development and compliance testing and optional customization services.

The Mobile Connectivity (MIPI) compliant IP cores are interface building blocks that simplify interconnect architectures in mobile platforms. This leads to smaller footprint, greater interoperability between mobile IP, chips and devices from diverse sources and lower power and Electro Magnetic Interface (EMI).

This document describes the Silicon Dreams IP Core that functions as a MIPI Camera Serial Interface (CSI-2 Combo) Receiver, which interfaces between a peripheral device (Camera module) and a host processor (baseband, application engine). The CSI-2 Combo Receiver IP communicates over a D-PHY (or) C-PHY serial link to image processing block, part of the application engine. The Silicon Dreams CSI-2 combo IP is MIPI compliance and provides a standard, scalable, low-power, high-speed interface that supports a wide range of higher image resolutions.

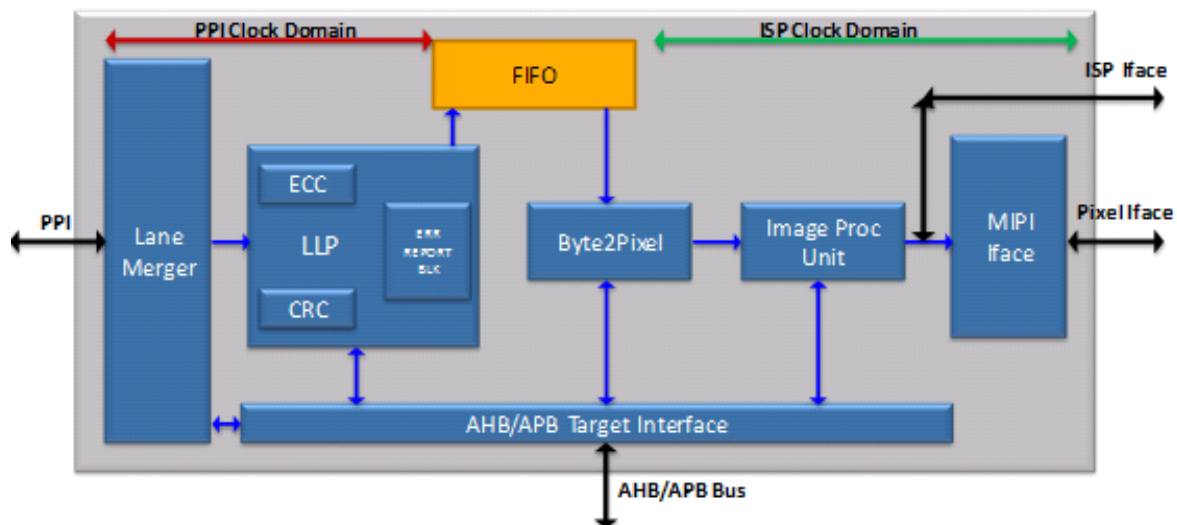


Figure 2 Functional Block Diagram

2.2 Features

- Compliant with the following MIPI specifications
 - CSI2 specification v1-3
 - DPHY specification v1-2
 - CPHY specification_v1-0
 - CSI-2 Combo Receiver Core features:
 - Use of either D-PHY/C-PHY by user configuration
 - Different Configuration allowed for multiple use cases,
 - 4-Lane/8-Lane D-PHY / 3-Lane C-PHY
 - Lane Configurability depending on the bandwidth requirements of the application, up to 8-lanes for DPHY and up to 3-lanes for C-PHY
 - High Speed (HS) receiver rates of 182Mbps to 5714Mbps per lane with C-PHY interface
 - High Speed (HS) receiver rates of 40Mbps to 2500Mbps per lane with D-PHY interface
 - Supports for Ultra Low Power Mode (ULPS)
 - Single (or) Optional Multi-Pixel mode interface to ISP. The multi-pixel mode is used in high bandwidth requirement applications to lower the ISP clock frequency requirement.
 - Optional Pixel Level Interface to ISP with HSYNC, VSYNC, DATA and DATA VALID
 - Streams the received pixels onto eight data channels(customizable) based on the channel configurability from ISP
 - Separate data channel for the short generic packets
 - Support for all packet level errors, Protocol Decoding Level errors
 - Support for cut-through (or) store and forward mode. Cut-through mode makes use of shallow Memory for memory critical applications.
 - Optional support for Compressed data formats
 - Optional support for different error counting
 - Pixel formats supported
 - RAW data type – RAW8, RAW10, RAW12, RAW14
 - YUV data type – YUV422-8bit, YUV422-10bit
 - RGB data type – RGB888, RGB666, RGB565, RGB555, RGB444
 - All user Defined data types / JPEG
 - Generic 8-bit long packet data types
 - Host interface for register configuration and monitoring,
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- Used for programming both CSI-2 and PHY related registers. Reserved address space [0x00 – 0x0F] for the PHY related registers.
 - Optional support for the AHB/APB Interface

2.3 IP Deliverables

- Verilog HDL of the IP Core
- User guide
- Synthesis scripts
- Link report
- CDC report
- Verilog test suite
- Gate count estimates available upon request