



Silicon Dreams
S I L I C O N T O T H E P O W E R O F Y O U R D R E A M S

D-PHY1.2/CPHY1.1 (2.5Gbps) and D-PHY2.5/CPHY2.0 (4.5Gbps) IP

Datasheet

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1. Introduction

Silicon Dreams is a provider of licensable Intellectual Property Cores for the Semiconductor industry along with software development and SoC design services.

Silicon Dreams was founded in 2022 to address the burgeoning semiconductor industry and its timing was well founded with the company's explosive growth along with the AI boom. The company is rapidly expanding its operations internationally to be closer to its customer base.

We have licensees Worldwide with most of our customers based in the USA followed by the APAC region with a significant presence in China and Japan.

Our goal is to enable customers to realize their dreams on silicon through our licensable intellectual property cores, design services and software.

The company can also build custom silicon per the customers specifications.

2. D-PHY1.2/CPHY1.1 (2.5Gbps)

2.1 Overview

The ever increasing demand for band width for the high resolution cameras resulted in to search for a simple, cost effective, rate efficient PHY which can support above 2.5Gbps. This search resulted into a new kind of PHY, which even at less channel rate provides very high data rate.

CPHY1.1 can achieve a very high data rate of 5.7Gbps per lane compared to the 2.5Gbps of DPHY1.2 and its legacy, still maintain the channel rate at 2.5Gsps which is same as CPHY1.1. CPHY achieves this by using a unique encoding mechanism in which 16 bit of input data is encoded into 7 symbols and each symbol is transmitted over a 3 Phase encoded line. With CPHY v1.1, the maximum channel rate achieved would be 3Gsps which would result in an effective data rate of 5.7Gbps.

Silicon Dream's ComPhy is a CPHY/DPHY combo universal PHY which can be configured both as Transmitter and Receiver. Silicon Dream's novel and innovative design techniques allowed sharing a number of modules between the CPHY and DPHY with no impact on performance resulting in optimal area and power.

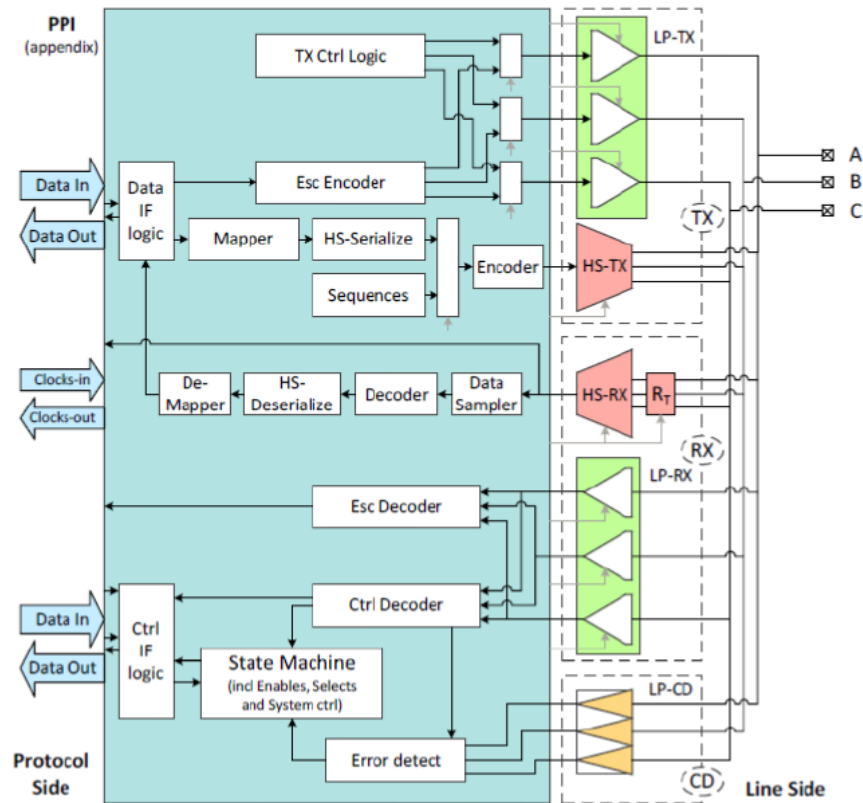


Figure 5 CPHY Lane Architecture

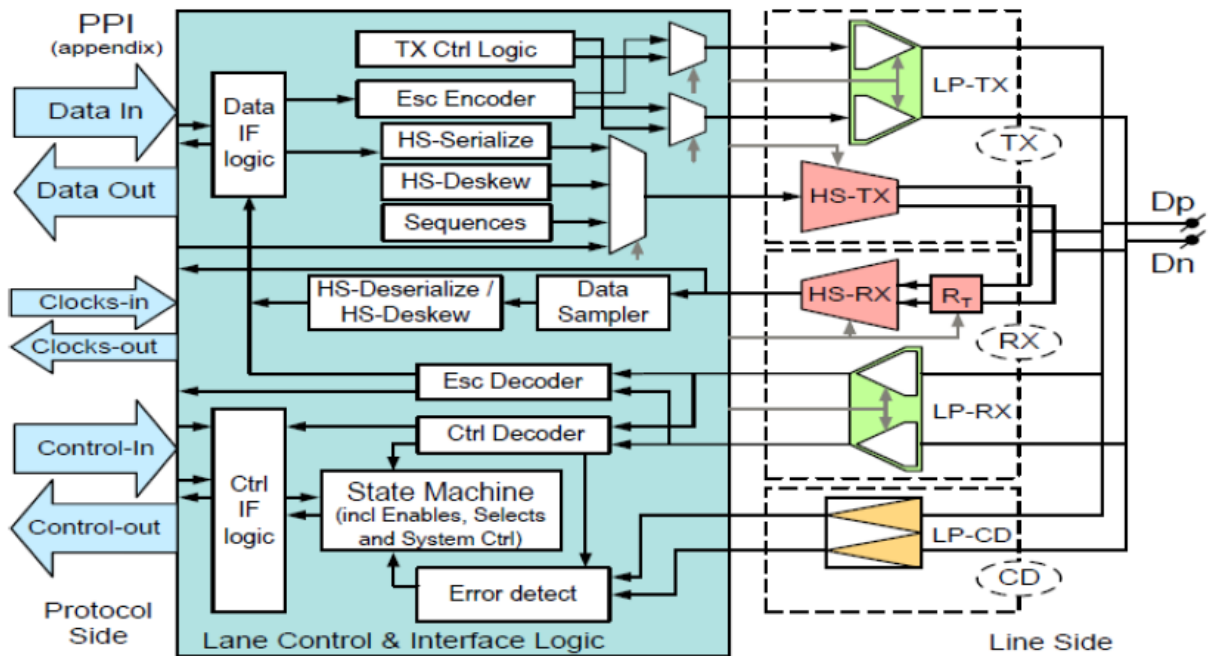


Figure 6 DPHY Lane Architecture

2.2 Features

- Compliant to DPHY 1.2 and CPHY 1.1
- Supports CSI2-1.3, DSI2-1.1
- Supports transfer at high speed mode with a bit rate of 182-5700Mbps for CPHY1.1
- Supports synchronous transfer at high speed mode with a bit rate of 40-2500Mbps for DPHY1.2
- Supports a channel rate of 2500Msps for CPHY
- CPHY/DPHY combo which can support both modes in same IP
- Supports asynchronous transfer at low power mode with a bit rate of 10 Mb/s
- Spaced one hot encoding for Low power [LP] data
- Supports up to one clock lane and four data lanes for DPHY1.2
- Three 3phase encoded data lanes for CPHY1.1
- Clock recovery mechanism from the data streams for the CPHY
- Same physical lines are used for both CPHY and DPHY
- 16 bit to 7 symbol mapper and 3phase encoder for CPHY
- DPHY and CPHY shares same design elements providing optimal design footprint
- Deskew support for the DPHY 1.2
- Supports error detection mechanism for sequence errors and contentions
- Supports ultra-low power mode, high speed mode and control mode.
- Has clock divider unit to generate clock for parallel data reception and transmission from and to the PPI
- Activates and disconnects high speed terminators for reception and transmission.
- Supports standard PHY transceiver compliant to MIPI Specification
- Supports standard PPI interface compliant to MIPI Specification for both DPHY1.2 and CPHY1.1
- Clock lane supports unidirectional communication
- On-chip clock generation configurable for either transmitter or loopback (BIST)
- PHY can be configured as a master or slave.
- Testability for Tx, Rx and PLL
- Built in Self Test for CPHY and DPHY
- Core is structured to increase the number of data lanes.
- Supports scan insertion and stitching for DFT
- Supports additional flexibility in terms of data lane/line polarity swapping
- Provides extensive debug capability and access which facilitate easy silicon debug and device characterization

2.3 Deliverables

- GDS-II
- CDL netlist for LVS
- LVS reports
- DRC and Antenna reports
- LIB files
- User guide and Integration Guides
- LEF
- Scan-inserted netlist for DFT
- Verification Environment with behavioral models
- IBIS Models

3. D-PHY2.5/CPHY2.0 (4.5Gbps)

3.1 Overview

The COMPHY is a semiconductor chip with Universal DPHY and CPHY functionalities that can interface with the Camera and Display interfaces; both transmit and receive, and is capable of meeting line rates of 4.5Gbps/lane in DPHY mode and 4.5Gbps/lane in CPHY mode (4.5Gbps short-haul). This product offers complete debug facilities to validate Application processors with MIPI interfaces, MIPI Cameras, and MIPI displays.

The COMPHY is predominantly a Combination PHY that combines the functionalities of the MIPI CPHY 2.0 and MIPI DPHY 2.5.

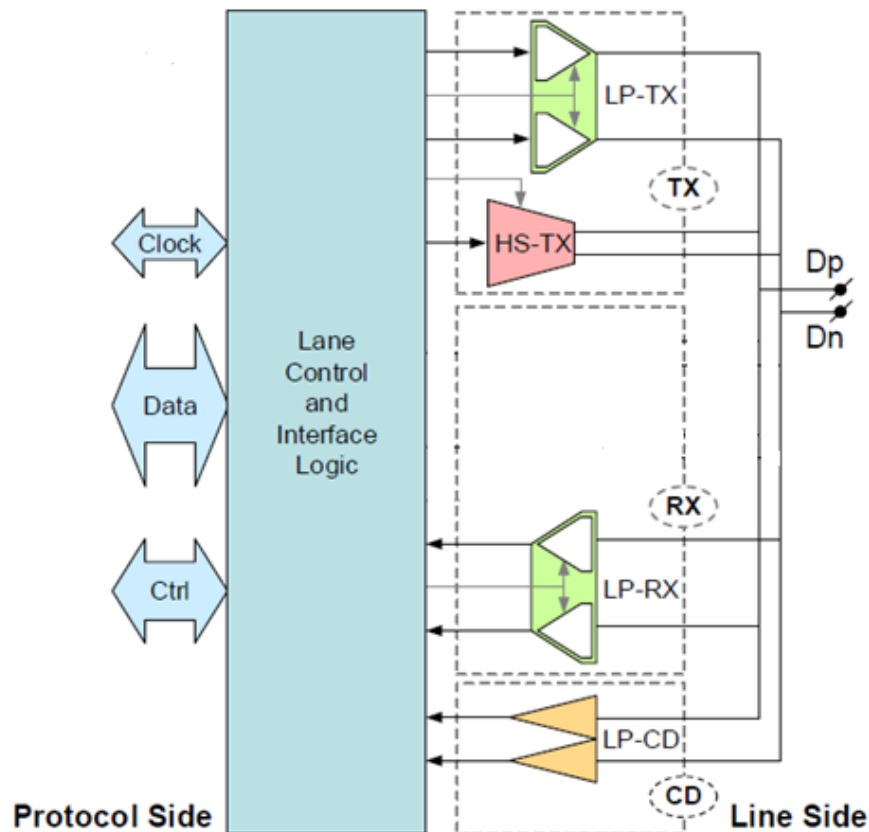


Figure 7 Block diagram of DPHY

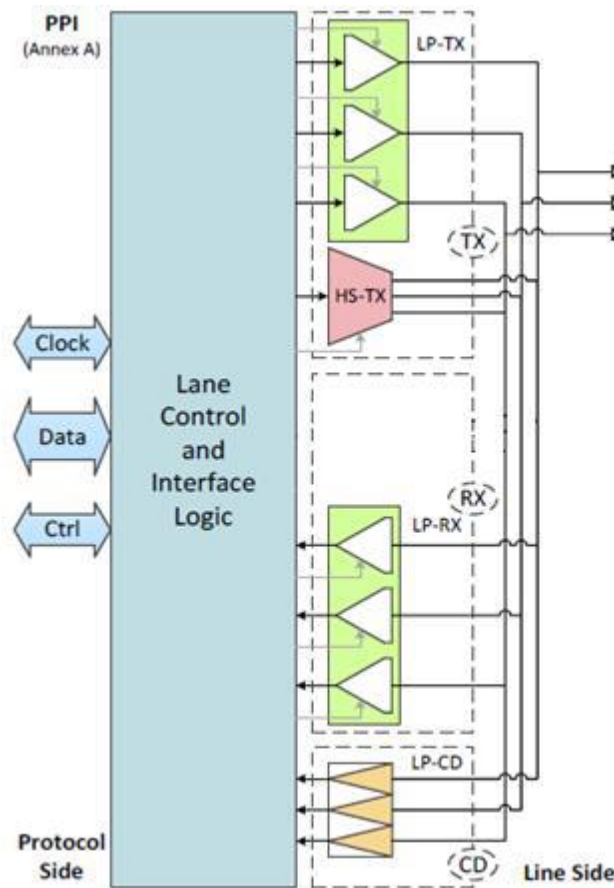


Figure 8 Block diagram of CPHY

3.2 D-PHY Features

- Compliant with MIPI Alliance Standard for D-PHY specification version 2.5
- Supports synchronous transfer at high-speed mode with a bit rate of 80-1500 Mb/s without skew calibration, up to 2500 Mb/s with skew calibration and up to 4500 Mb/s with equalization
- Supports asynchronous transfer at low power mode with a bit rate of 10 Mb/s
- Spaced one hot encoding for Low power [LP] data
- Supports one clock lane and four data lanes
- Supports LP contentions in data lanes
- Support transfer of data in high-speed mode
- Supports ultra-low power mode, alternate low power, high-speed mode and control mode

- Supports standard PPI interface compliant to MIPI Specification Clock Lane
- Supports unidirectional communication
- Support for BIST methodology as per the CPHY2.0 standard and is extended to DPHY
- PHY can be configured as a master
- Support "HS Skew" and "Alternate Calibration Sequence"
- Support for "Preamble sequence"
- Supports for polarity swap for all lanes
- APB register access to all COMPHY TX registers
- Support SCAN and BIST modes

7.3 C-PHY Features

- Compliant with MIPI Alliance Standard for C-PHY specification version 2.0
- Supports asynchronous transfer at high-speed mode with a symbols rate of 80-1300 MS/s for long channel without equalization and 2300MS/s with equalization. For standard reference channel it is 1700 MS/s without equalization and 3500 MS/s with equalization. For short channel it is 2500 MS/s and 4500 MS/s respectively
- Support for Calibration sequence
- Supports asynchronous transfer at low power mode with a bit rate of 10 Mb/s
- Spaced one hot encoding for Low power [LP] data
- Supports maximum of three data lanes
- Supports error detection mechanism for sequence errors and contentions
- Data lanes support transfer of data in high-speed mode
- Supports ultra-low power mode, alternate low power, high-speed mode and control mode
- Supports standard PPI interface compliant to MIPI Specification
- PHY can be configured as a master
- Supports High speed mode in Forward communication
- Supports BIST features covered in the CPHY2.0 Spec
- APB Slave register access to all COMPHY TX registers
- Support SCAN and BIST modes

7.4 Deliverables

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- CDL netlist for LVS
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